

An Efficient Diode Clamped Multilevel Inverter for Reducing THD with Selective Harmonic Elimination Pulse Width Modulation (SHEPWM)

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Abstract: Selective harmonic elimination pulse width modulation (SHEPWM) technique is applied to diode clamped multi-level inverter (DCMLI) to reduce total harmonic distortion (THD) and improve the quality of output power. The modulation technique is implemented centered on dog leg optimization method to find the optimized values for switching angles (θ) of switches (IGBTs) employed. Twelve level diode clamped inverter is implemented in Matlab and the results are compared with non-optimized switching angles also 5-level DCMLI using SHEPWM is compared with other modulation techniques.

Keywords: DCMLI, Dog Leg Method SHEPWM, Switching Angles, THD.

1. INTRODUCTION:

Economic development and fast growth in world population has increased the demand of energy and global warming. Renewable energies like solar and wind etc. are green, clean and cheap sources of energy and a solution of environment pollution and energy demand issues [1].

Various modulation techniques e.g. SPWM, SVPWM are implemented to reduce harmonics and improve output power quality [1]. Similarly numerous types of multi-level inverters are used for the purpose of reduction in harmonics and improvement in power quality [2]. One of the multilevel inverter implemented for power improvement is 5-Level inverter (cascaded) using DSTATCOM [3]. Chopper with flying capacitor used in DCMLI for the reduction of stress and produces AC voltage of multilevel [4]. Based on twelve switches a DCMLI (5-levels) for the machines running on higher speed [5]. 3-level DCMLI with ANPC, ZCT used for sustainable energy [6]. Building H-Bridge for AC to DC conversion with the use of capacitors and single DC source with less harmonics [7]. Using different voltage balancing equations and techniques to form a flying capacitor H-Bridge multilevel inverter [8]. Cascaded inverters with particle swarm optimization technique to improve power quality and reduce total harmonics [9]. Cascaded inverter using SVPWM to minimize harmonics and switching frequency [10]. Many multi-level inverters are used but diode clamped multi-level inverter (DCMLI) is employed for many applications like power drives & utility system [11].

In this proposed method diode clamped 12-level inverter is implemented using selective harmonic elimination pulse width modulation technique (SHEPWM) to reduce the total harmonic distortion of the output wave form and improve quality of output. Optimization technique dog leg is used for switching angles of insulated gate bipolar transistors (IGBTs) employed in

the system. This method has less computation time and rectified results.

2. METHODOLOGY

12 level diode clamped multilevel inverter (DCMLI) with four sub-systems connected to DC batteries sources and switches state controller (SSC) is shown in fig.01. It consists of specific number of diodes, switches (IGBT's) and DC sources. The components required are calculated using equations 1, 2, 3. The total number of voltage levels (m) are counted in half cycle i.e. from $0-\pi$.

$$\text{Number of IGBTs} = 4 \left[\left(\frac{m}{2} \right) - 1 \right] \quad (1)$$

$$\text{Number of IGBTs} = 44$$

$$\text{Number of clamping diodes} = \left\{ \left(\frac{m}{2} \right) - 1 \right\} * \left\{ \left(\frac{m}{2} \right) - 2 \right\} \quad (2)$$

$$\text{Number of clamping diodes} = 110$$

$$\text{Number of batteries} = \left(\frac{m}{2} \right) - 1 \quad (3)$$

$$\text{Number of batteries} = 11$$

Fig 02 shows subsystem1 of 12 levels DCMLI which is connected in series with subsystem2 to complete first leg as there are two legs in this system. Second leg is similar to first leg, both first and second legs are connected to form a full H-Bridge DCMLI.

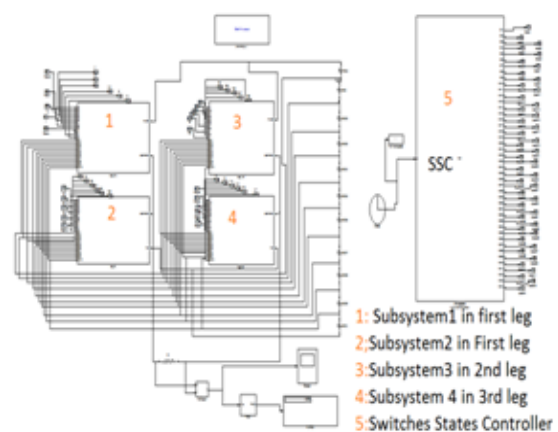


Fig01:12 Levels DCMLI

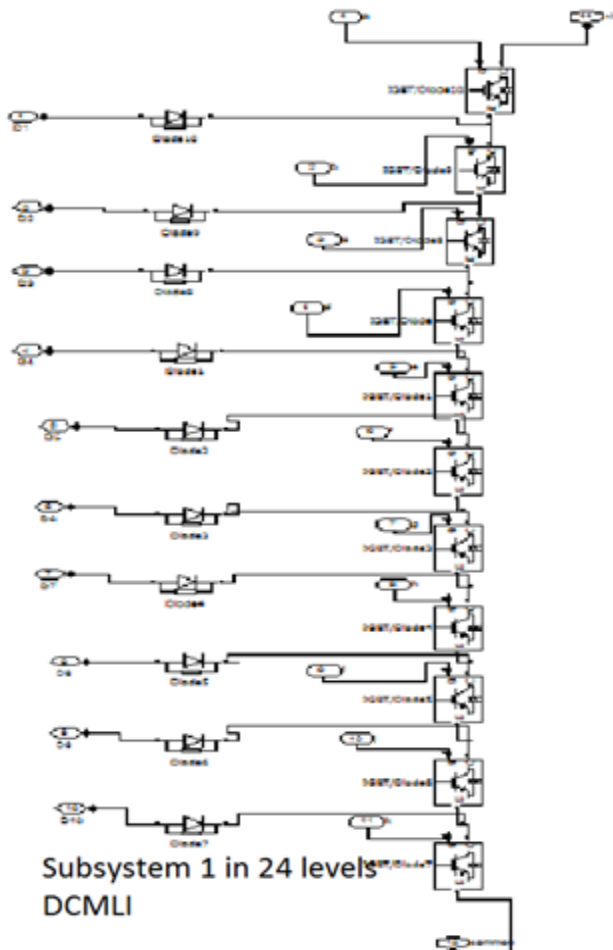


Fig 02: subsystem of 12 DCMLI

Stepped Voltages	Conducting Switches	Non Conducting Switches
0Vdc	12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33	1 2 3 4 5 6 7 8 9 10 11 34 35 36 37 38 39 40 41 42 43 44
1Vdc	11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32	1 2 3 4 5 6 7 8 9 10 33 34 35 36 37 38 39 40 41 42 43 44
-	-	-
-	-	-
-	-	-
10Vdc	2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23	1 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44
11Vdc	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22	23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44

Table 01: IGBTs Switching Pattern for 12 DCMLI

3. WORKING:

A table 01 shows the number of on and off switches for multi levels of output voltage from 0° to 90° 12 levels DCMLI's. At any level number of on switches = (m/2)-1 while each switch is turned on once at a time. The output of 12-DCMLI is a stepped waveform as shown in fig.3A for each step IGBT is switched at an angle such that the total harmonic distortion is reduced. To get a desired value of fundamental component of voltage and reduced THD, Selective harmonic elimination PWM method is used. Selective Harmonic elimination (SHE PWM) is used for low switching frequency and removing lower order odd harmonics such as 3rd, 5th, 7th, 11th and 13th. This method further uses of iterative optimization technique 'trust region dogleg' algorithms to compute switching angles (θ).

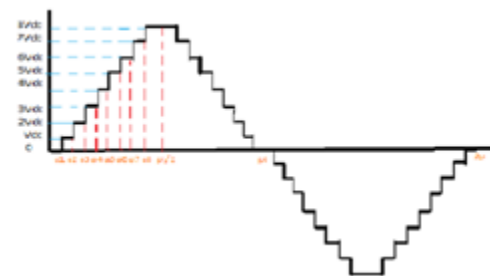


Fig 03 A: Stepped output of Diode Clamped 12- Level Inverter

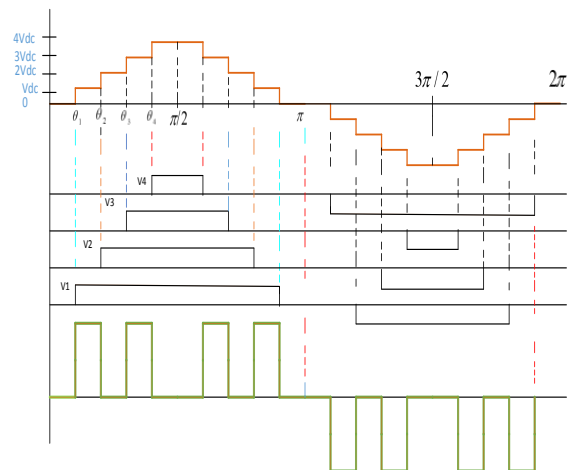


Fig 03 B: Stepped output of Diode Clamped 5- Level Inverter

4. MATHEMATICS:

Equations of the output voltage of DCMLI, peak values of harmonics for the calculation of THD and the system of non-linear equations for switching angles calculation are derived from Fourier series. Fourier series for a periodic function is expressed as

$$f_t = a_v + \sum_{n=1}^{\infty} a_n \cos(2\pi n f_o t) + b_n \sin(2\pi n f_o t) \quad (1)$$

Here a_v , a_n and b_n are the Fourier series coefficients and f_o is the fundamental frequency. Following relationships determine the values of these coefficients

$$a_v = \frac{1}{T} \int_{t_o}^{t_o+T} f(t) dt \dots\dots\dots(2)$$

$$a_n = \frac{2}{T} \int_{t_o}^{t_o+T} f(t) \cos(2\pi n f_o t) dt \dots\dots\dots(3)$$

$$b_n = \frac{2}{T} \int_{t_o}^{t_o+T} f(t) \sin(2\pi n f_o t) dt \dots\dots\dots(4)$$

Where t_o = Chosen time reference, T = Fundamental period.

For a signal having odd quarter wave Symmetry, Fourier series coefficients are given as

$$a_v = 0 \dots\dots\dots(5)$$

$$a_n = 0 \text{ for all } n \dots\dots\dots(6)$$

$$b_n = 0 \text{ for } n \text{ even} \dots\dots\dots(7)$$

$$\text{And } b_n = \frac{8}{T} \int_0^{T/4} f(t) \sin(2\pi n f_o t) dt \text{ for odd } n \dots\dots\dots(8)$$

The Multilevel inverter has odd quarter wave symmetry. Using Fourier coefficient equations of a quarter waves, Fourier coefficients for a DCMLI output are derived in terms of switching angles. Five angles are considered here only for mathematical calculations.

$$b_n = \frac{4}{\pi} \int_0^{\pi/2} f\left(\frac{\omega t}{2\pi f_o}\right) \sin(n\omega t) d(\omega t) \text{ for } n \text{ odd} \dots\dots\dots(9)$$

$$b_n = \int_{\theta_1}^{\theta_2} \frac{4}{\pi} (v_{dc}) \sin(n\omega t) d(\omega t) + \int_{\theta_2}^{\theta_3} \frac{4}{\pi} (2v_{dc}) \sin(n\omega t) d(\omega t) \\ + \int_{\theta_3}^{\theta_4} \frac{4}{\pi} (3v_{dc}) \sin(n\omega t) d(\omega t) + \int_{\theta_4}^{\theta_5} \frac{4}{\pi} (4v_{dc}) \sin(n\omega t) d(\omega t) \\ + \int_{\theta_5}^{\pi/2} \frac{4}{\pi} (5v_{dc}) \sin(n\omega t) d(\omega t)$$

where $\theta_1, \theta_2, \theta_3, \theta_4$ and θ_5 are the switching angles

Solving Integration results

$$b_n = \frac{4}{\pi} \int_0^{\pi/2} f\left(\frac{\omega t}{2\pi f_o}\right) \sin(n\omega t) d(\omega t) \text{ for } n \text{ odd}$$

$$b_n = -\frac{4}{\pi n} v_{dc} [\cos(n\omega t)]_{\theta_1}^{\theta_2} - \frac{4}{\pi n} (2v_{dc}) [\cos(n\omega t)]_{\theta_2}^{\theta_3} \\ - \frac{4}{\pi n} (3v_{dc}) [\cos(n\omega t)]_{\theta_3}^{\theta_4} - \frac{4}{\pi n} (4v_{dc}) [\cos(n\omega t)]_{\theta_4}^{\theta_5} \\ - \frac{4}{\pi n} (5v_{dc}) [\cos(n\omega t)]_{\theta_5}^{\pi/2} - \frac{4}{\pi n} (2v_{dc}) [\cos(n\omega t)]_{\theta_5}^{\pi/2} \dots\dots\dots(10)$$

$$= \frac{4}{\pi n} v_{dc} [\cos(n\theta_1) - \cos(n\theta_2)] + \frac{4}{\pi n} (2v_{dc}) [\cos(n\theta_2) - \cos(n\theta_3)] \\ + \frac{4}{\pi n} (3v_{dc}) [\cos(n\theta_3) - \cos(n\theta_4)] + \frac{4}{\pi n} (3v_{dc}) [\cos(n\theta_4) - \cos(n\theta_5)] \\ \dots\dots\dots(11)$$

when n is an odd integer

$$\cos\left(n \frac{\pi}{2}\right) = 0$$

$$b_n = \frac{4}{\pi n} v_{dc} [\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cos(n\theta_4) + \cos(n\theta_5)] \dots\dots\dots(12)$$

Equation 12 provides peak values of odd harmonics in a DCMLI which can be used to calculate total harmonic distortion (THD) using equation 13.

$$\dots\dots\dots(13)$$

$v_1, v_2, v_3, \dots, v_n$ are the peak values of harmonics Using resultant theory, a set of non-linear equations is derived from equation 12 which can be solved for the values of angles. In case of 12 levels DCMLI, following set of equations is obtained to eliminate 3rd, 5th, 7th, 9th and 11th harmonics.

$$\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) + \dots\dots\dots\cos(3\theta_{11}) = 0 \\ \dots\dots\dots(14)$$

$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \dots\dots\dots\cos(7\theta_{11}) = 0 \\ \dots\dots\dots(15)$$

$$\cos(9\theta_1) + \cos(9\theta_2) + \cos(9\theta_3) + \dots\dots\dots\cos(\theta_{11}) = 0 \\ \dots\dots\dots(16)$$

$$\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \dots\dots\dots\cos(11\theta_{11}) = 0 \dots\dots\dots(17)$$

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \dots + \cos(\theta_{11}) = \frac{mM\pi}{4} \dots (18)$$

$$M = \frac{v_1}{v} \dots (19)$$

$$m = (\text{number of levels}/2) - 1 \dots (20)$$

Switching angles are calculated with the help of MATLAB program using trust region dogleg algorithm (shown in fig 04) for a range of modulation indexes. Table 02 angles are calculated when equation 21 is satisfied.

$$0 \leq \theta_1 \leq \theta_2 \leq \theta_3 \leq \theta_4 \leq \theta_5 \leq \theta_6 \leq \theta_7 \leq \theta_8 \leq \theta_9 \leq \theta_{10} \leq \theta_{11} \dots (21)$$

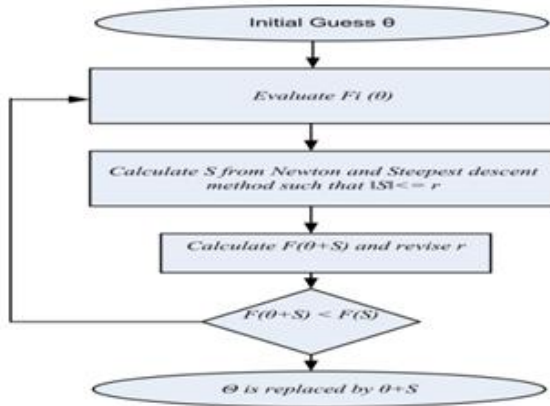


Fig04: Dog Leg Algorithm

Where θ is an array containing initial guess for $\theta_1 + \theta_2 + \dots + \theta_n$

$$F(\theta) = \sum_{i=1}^n [F_i(\theta)]^2 \dots (22)$$

S is correction step, r = radius of trust region

Figure shows the flow chart of trust region dogleg method for computing $\theta_1 + \theta_2 + \dots + \theta_n$ from set of functions $f_1, f_2, f_3, \dots, f_n$

In first step, a correction step is calculated and added to the initial guess. Dogleg utilizes Newton and steepest descent methods. The combination of these two methods ensures a fast convergence and a solution of function in the steepest descent direction. The second step involves finding the value of trust region radius to estimate length of step for the current iteration such that the following condition is obeyed.

$$F(\theta + s) < F(\theta) \dots (23)$$

Third step performs a check the new values of function. Has the function minimized,

If Yes replace θ by $\theta + S$

If not, go for the next iteration.

M	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6
0.95	0.0541	0.1463	0.2461	0.3331	0.4356	0.5740
0.9	0.0000	0.1502	0.2408	0.3593	0.4916	0.6036
0.85	0.0000	0.1731	0.2623	0.4003	0.4934	0.6137
0.8	0.0000	0.1694	0.3155	0.3906	0.5308	0.6896
0.75	0.0000	0.1870	0.3287	0.4196	0.5761	0.7428
0.7	0.0000	0.2499	0.2826	0.4834	0.6322	0.7779

θ_7	θ_8	θ_9	θ_{10}	θ_{11}
0.6757	0.7713		0.9824	1.1195
0.7106	0.8380		1.0304	1.3253
0.8056	0.8958		1.1659	1.4188
0.8212	1.0237		1.2916	1.4870
0.8929	1.1568		1.4078	1.5424
0.0296	1.2290		1.4645	1.5617

Table 02: Optimized switching angles in radians for 12 level DCMLI

5. EXPERIMENTAL RESULTS

Experimental results are obtained for optimized switching angles using dog leg method and for non-optimized IGBTs switching angles of 12-level DCMLI. 5-level DCMLI results are taken for optimized switching angles and experimental results show

- Values of total harmonic distortion
- Harmonic order of harmonics with reference to fundamental component
- Effect of modulation index on THD.

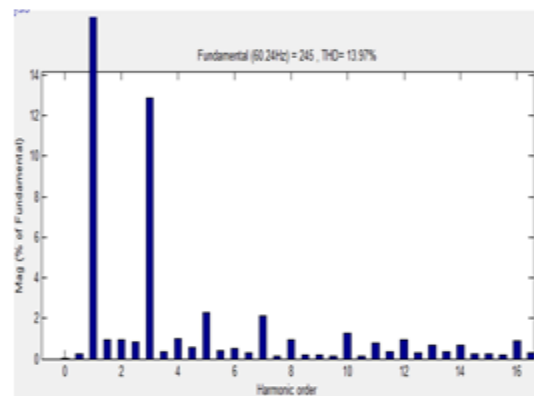


Fig 05 THD and frequency spectrum of 12 levels DCMLI with non-optimized angles

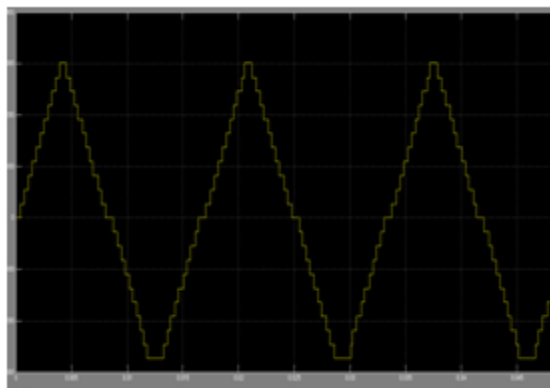


Fig 6 voltage wave form of 12 level DCMLI non-optimised $m=0.95$

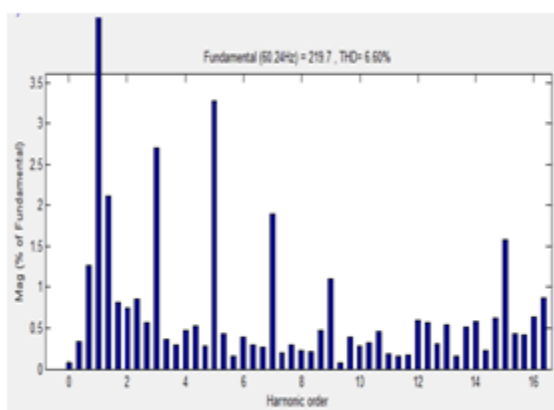


Fig 07 THD and frequency spectrum of 12 levels DCMLI with optimized angles

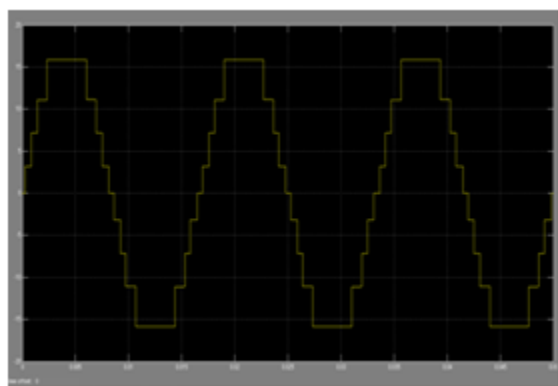


Fig 08 voltage wave form of 12 level DCMLI optimised And $m=0.7$

M	THD
0.95	3.80
0.9	4.80
0.85	5.65
0.8	5.80
0.75	6.12
0.7	6.49

Fig 9 THD values of 12-DCMLI for different modulation index (m)

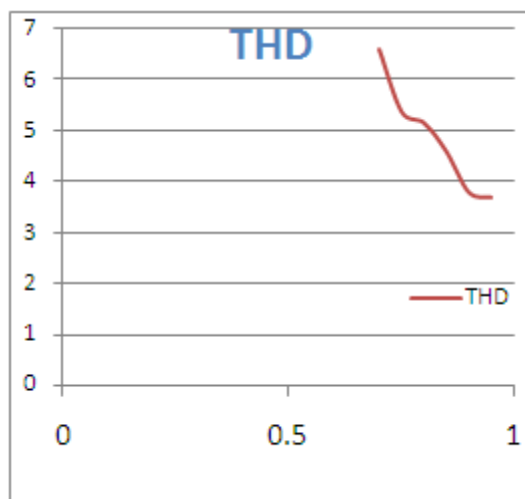


Fig 10 THD VS modulation index (m)

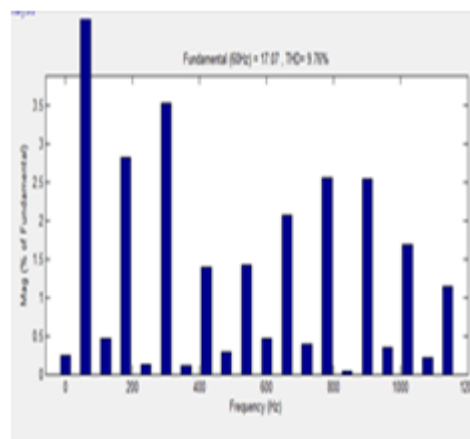


Fig11 THD and Frequency spectrum of 5-levels DCMLI with optimized angles ($m=0.95$)

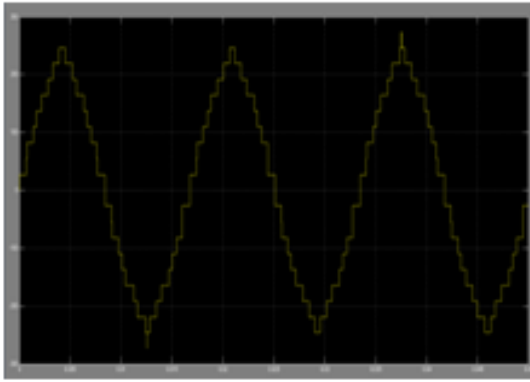


Fig12 Voltage Waveform of 5- Level DCMLI optimized and $m=0.95$

Below table shows a comparison of various techniques employed for 5-level diode clamped inverter to reduce total harmonic distortion (THD). Modulation techniques like PWM, POD-PWM, SPWM, Third harmonic injection, offset voltage and trapezoidal are used but proposed technique in this paper improves output voltage waveform with lowest THD value and power factor value near to 1.

No.	Modulation Technique	%THD
1	POD-PWM[12]	32.32
2	SPWM [13]	16.97
3	Third harmonic injection[13]	17.03
4	Offset voltage [13]	16.38
5	Trapezoidal [13]	18.39
6	Three harmonic Injection[14]	17.57
7	SPWM[15]	16.82
8	PWM[16]	10.68
9	Proposed Technique (SHEPWM) With Dog Leg Method	9.76

Table3: THD Values of 5-Level diode clamped inverters for different modulation techniques ($m=0.9$)

6.CONCLUSION

Selection harmonic elimination pulse width modulation technique (SHEPWM) has greatly reduced total harmonic distortion and improved output voltage waveform. Compared to other techniques applied to diode clamped multi-level inverters (DCMLI) the proposed SHEPWM technique based dog leg optimization technique has the lowest THD value, better output power and voltage waveform. Increasing modulation index (m) reduces the harmonics and improves power quality. The proposed system (DCMLI) is best option for industrial applications like induction motors.

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